

Fig. 1a

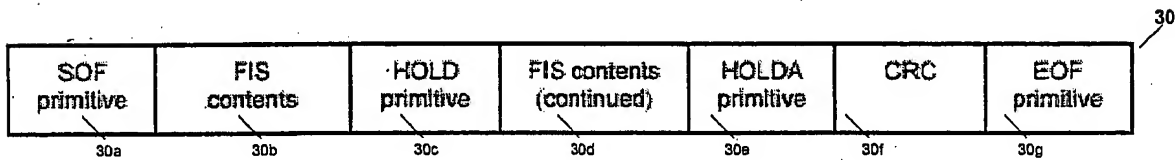


Fig. 1b

				Register access operation	
				Read	Write
				Data Port 31da	
				Error 31e	Features 31f
				Sector Count [15:8], [7:0] 31ga	
				Sector Number [31:24], [7:0] 31gb	
				Cylinder Low [39:32], [15:8] 31gc	
				Cylinder High [47:40], [23:16] 31gd	
				Device / Head 31de	
				Status 31e	Command 31e

Fig. 1c

0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)	40(i)
1	Dev / Head	Cyl High				Cyl Low	Sector Number	
2	Features (exp)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp)	
3	Control	Reserved (0)				Sector Count (exp)	Sector Count	
4	Reserved (0)	Reserved (0)				Reserved (0)	Reserved (0)	

Fig. 1d(i) Register FIS Host to Device

0	Error	Status	R	I	R	Reserved (0)	FIS Type (34h)	40(ii)
1	Dev / Head	Cyl High				Cyl Low	Sector Number	
2	Reserved (0)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp) (0)	
3	Reserved (0)	Reserved (0)				Sector Count (exp)	Sector Count	
4	Reserved (0)	Reserved (0)				Reserved (0)	Reserved (0)	

Fig. 1d(ii) Register FIS Device to Host

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (39h)	40(iii)
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Fig. 1d(iii) DMA Activate FIS, Device to Host

0	Reserved (0)	Reserved (0)	A	I	D	Reserved (0)	FIS Type (41h)	40(vi)
1		0					TAG	
2		0						
3		Reserved (0)						
4		DMA Buffer Offset						
5		DMA Transfer Count						
6		Reserved (0)						

Fig. 1d(iv) DMA Setup FIS

0	Error	R	Status Hi	R	Status Lo	R	I	R	Reserved (0)	FIS Type (A1h)	40(v)
1									SActive 31:0	41	

Fig. 1d(v) Set Device Bits FIS

0	Error	Status	R	I	D	Reserved (0)	FIS Type (5Fh)	40(vi)
1	Dev / Head	Cyl High				Cyl Low	Sector Number	
2	Reserved (0)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp) (0)	
3	E_Status	Reserved (0)				Sector Count (exp)	Sector Count	
4	Reserved (0)				Transfer Count			

Fig. 1d (vi) PIO Setup FIS

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)	40(vii)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)							
...								
n								

Fig. 1d (vii) Data FIS

0	Reserved (0)	Pattern Definition	R	R	R	Reserved (0)	FIS Type (58h)	40(viii)
		T A S L F P R V						
1	Data [31:24]	Data [23:16]	Data [15:8]		Data [7:0]			
2	Data [31:24]	Data [23:16]	Data [15:8]		Data [7:0]			

Fig. 1d(viii) BIST Activate FIS

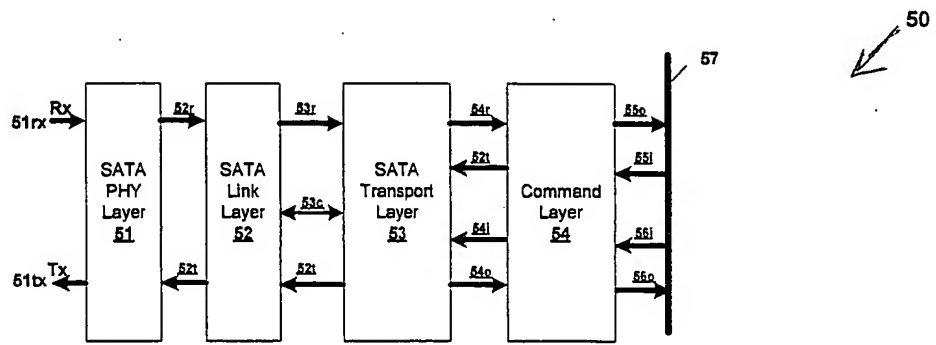


Fig. 2a

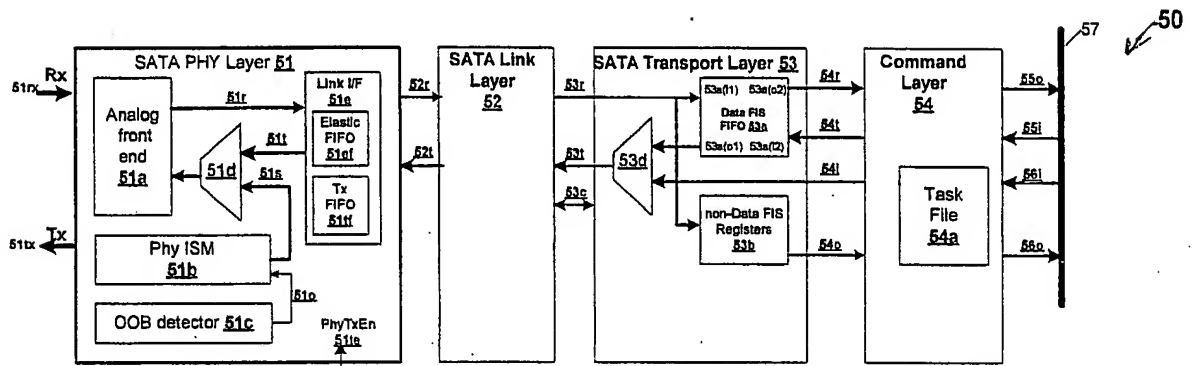


Fig. 2b

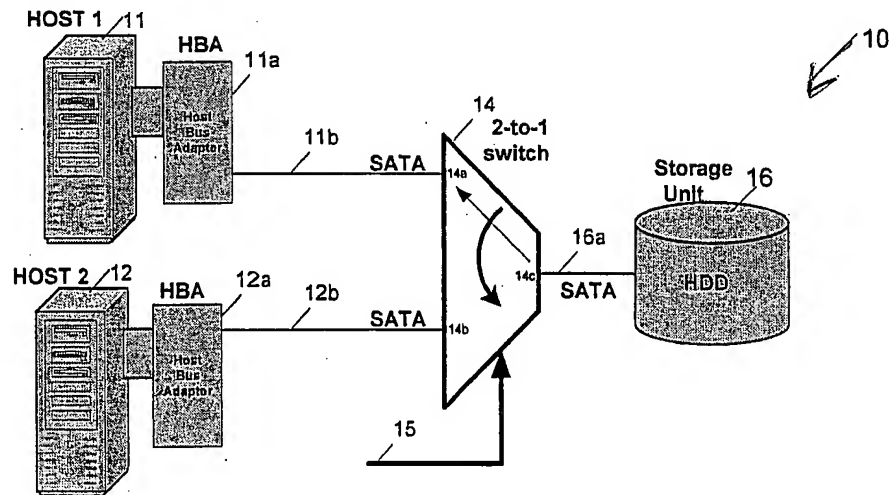


Fig. 3a

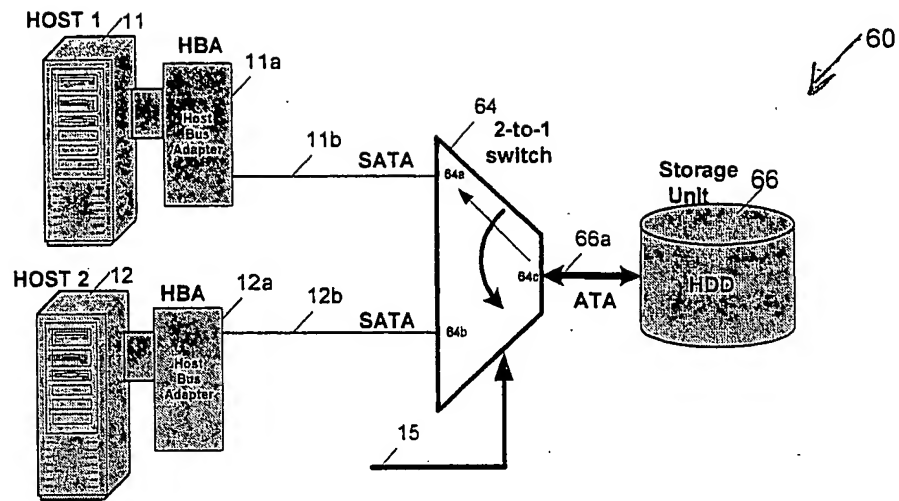


Fig. 3b

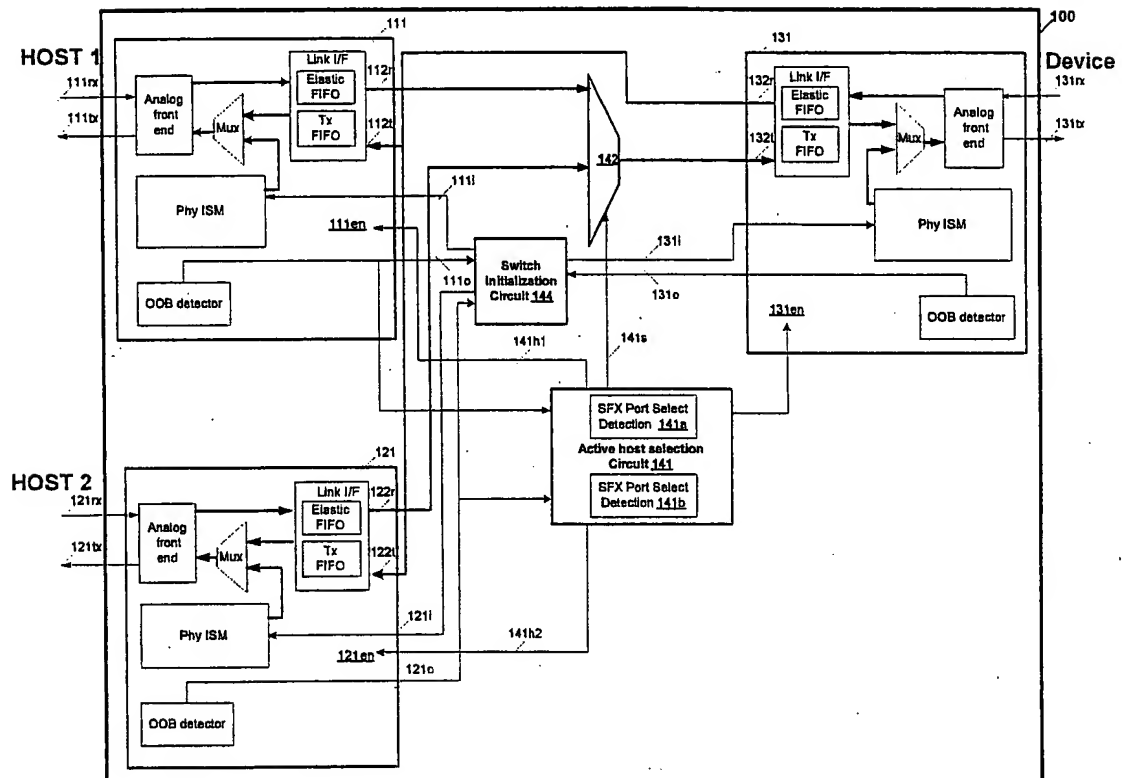
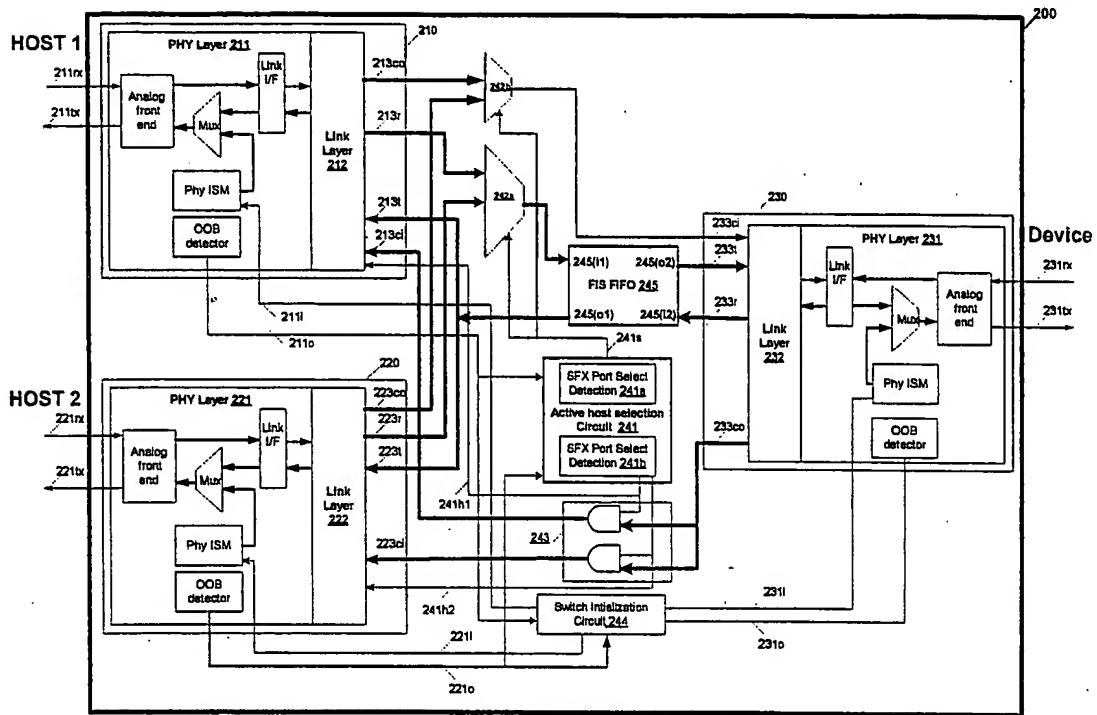
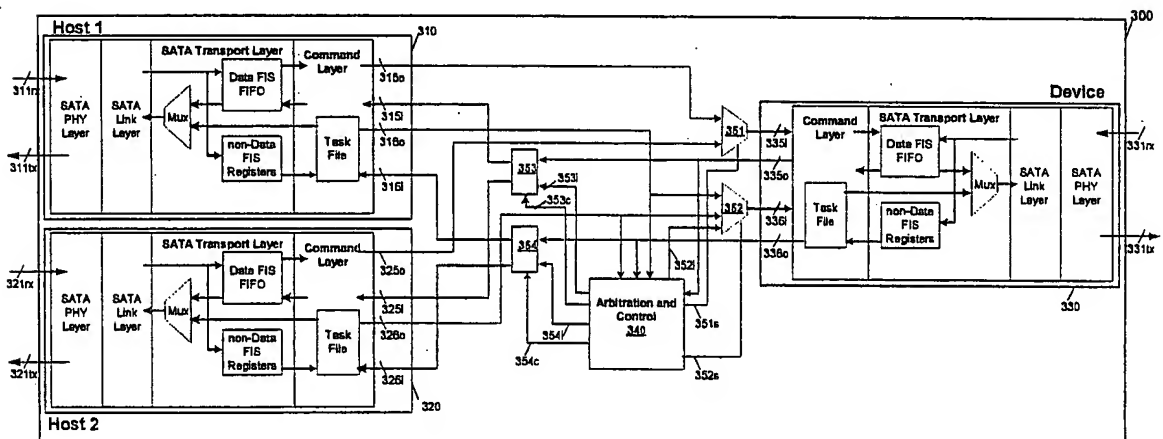


Fig. 4



**Fig. 5**



**Fig. 6**

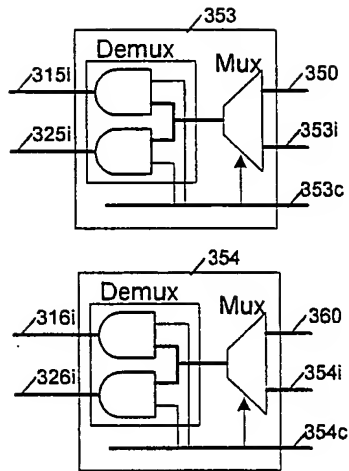


Fig. 7c

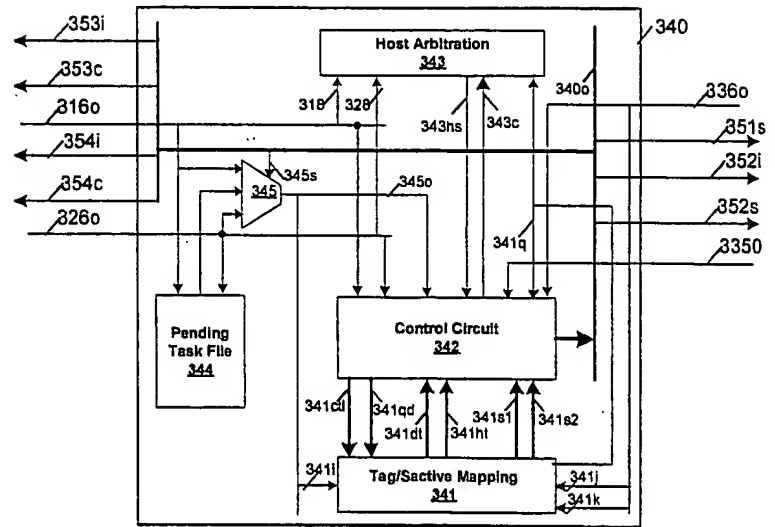


Fig. 7a

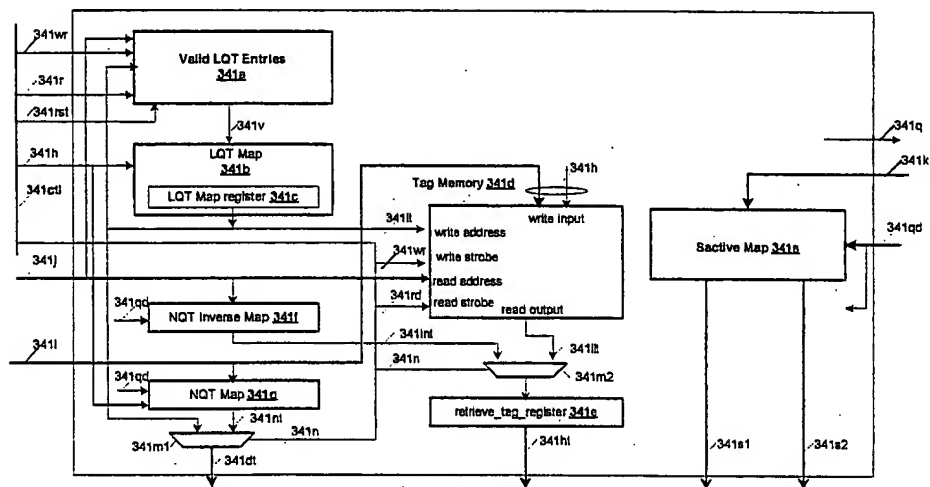


Fig 7b

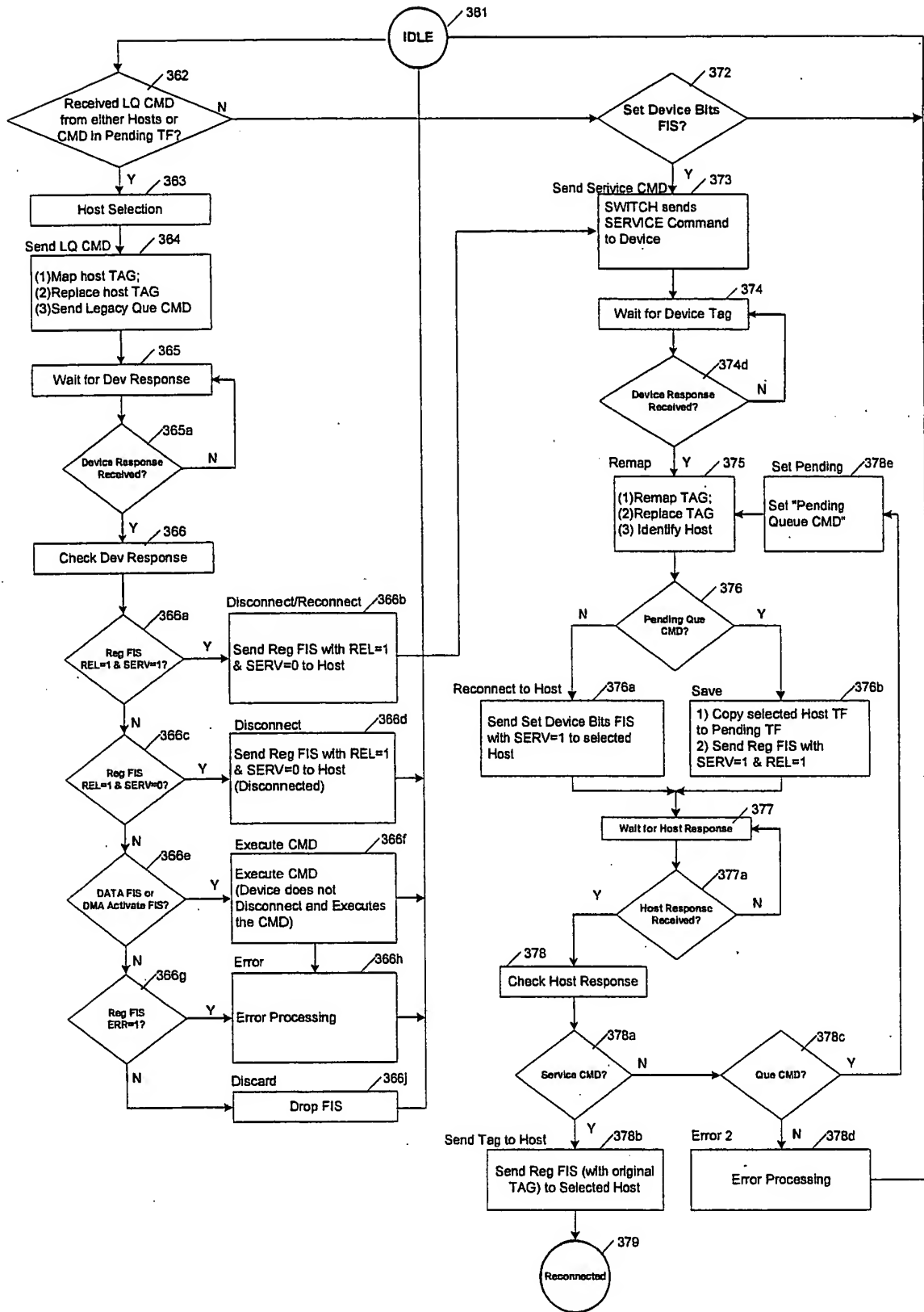


Fig 8a



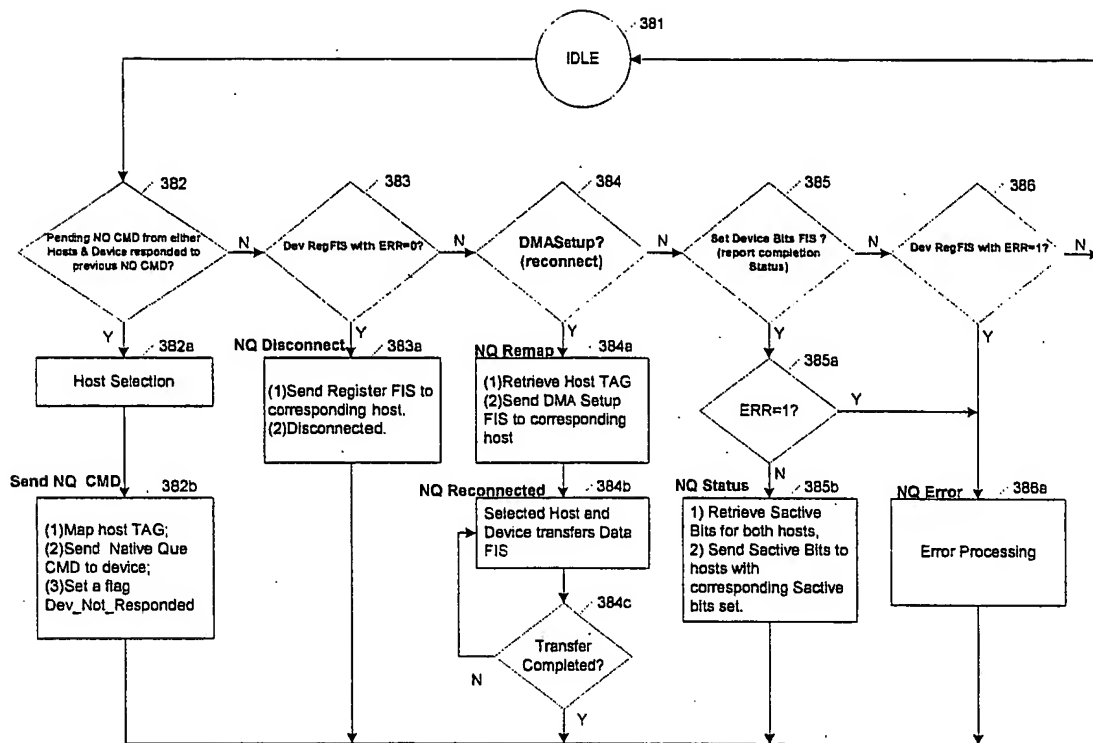
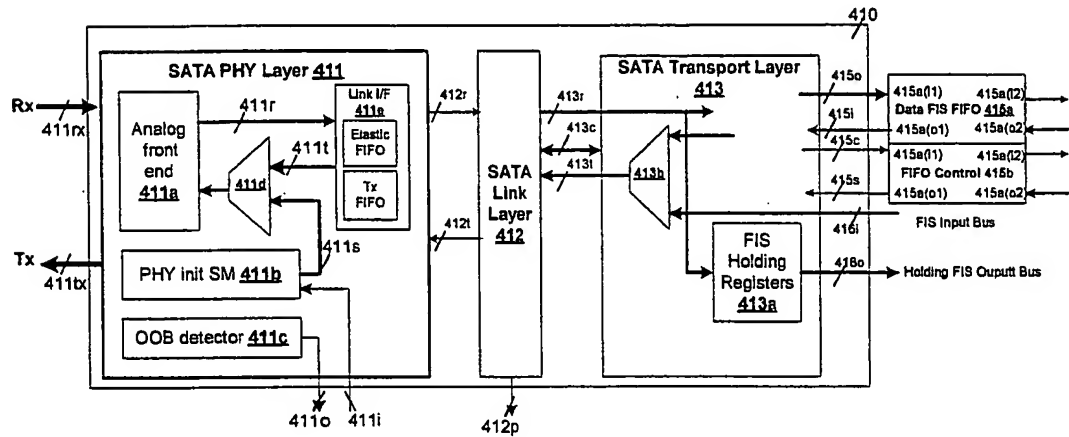
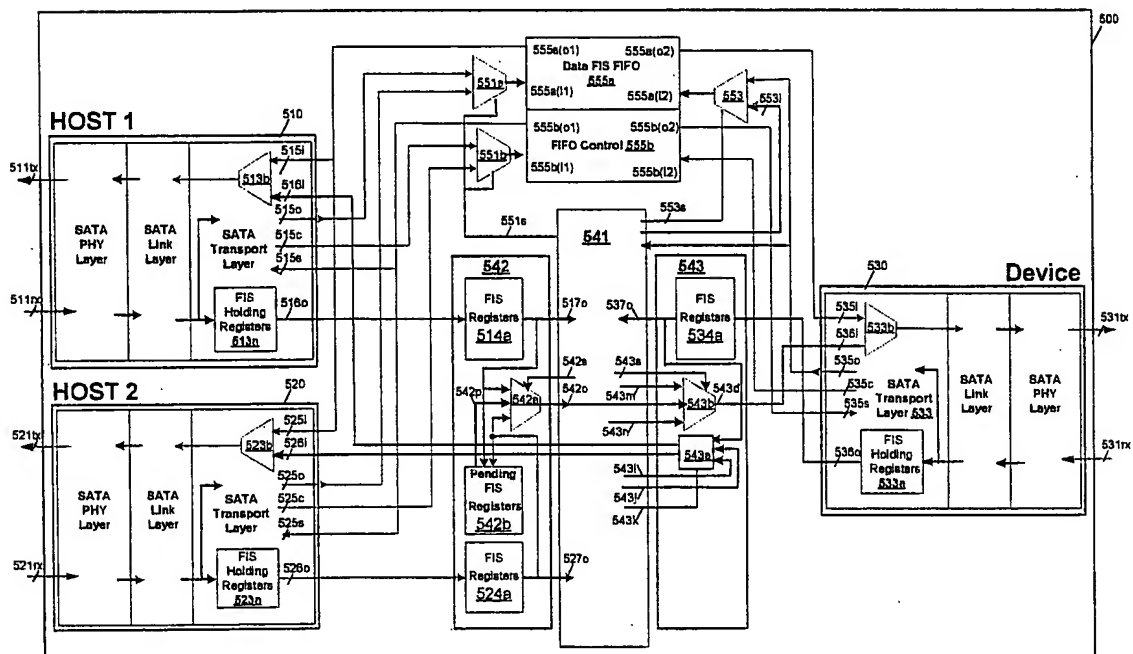


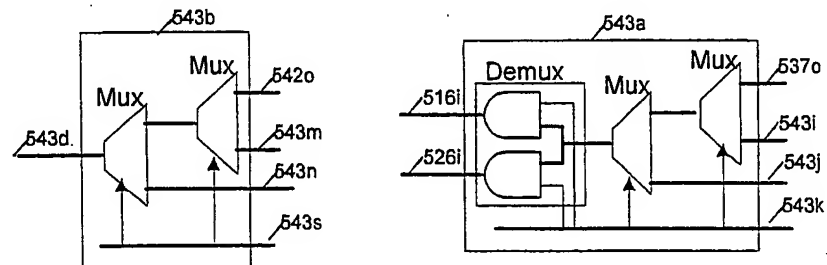
Fig 8b



**Fig. 9**



*Fig. 10a*



*Fig. 10c*

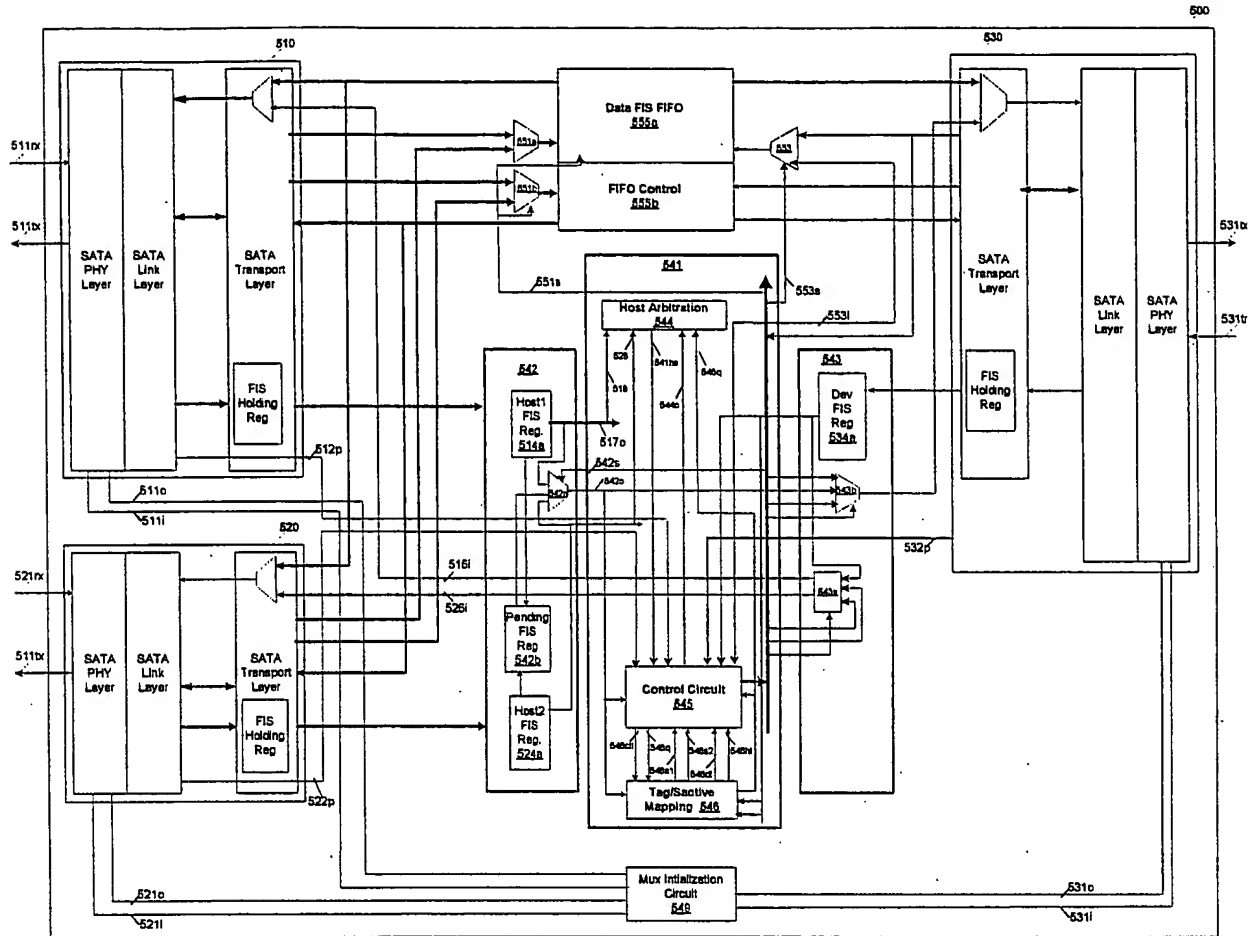


Fig. 10b

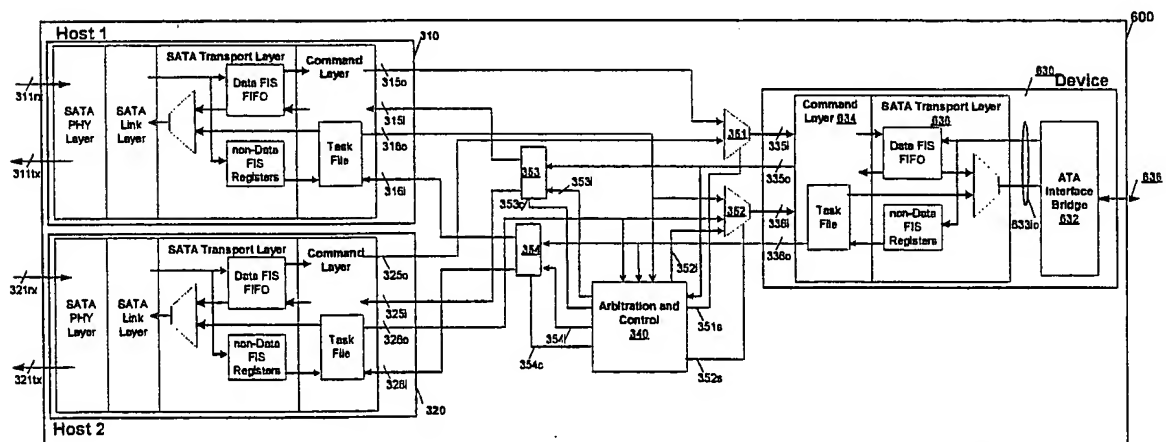


Fig. 11a

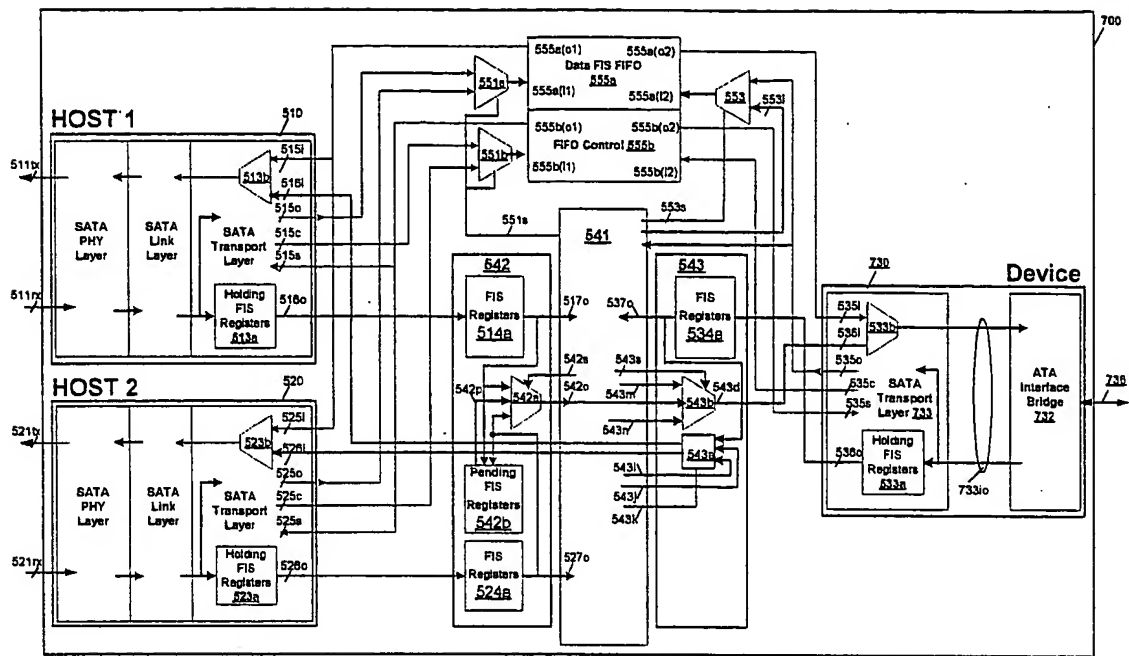


Fig. 11b

	H-bit 91(0)																							
0	Features					Command					C	R	R	Reserved (0)					FIS Type (27h)					90(1)
1	Dev / Head					Cyl High					Cyl Low					Sector Number								
2	Features (exp)					Cyl High (exp)					Cyl Low (exp)					Sector Num (exp)								
3	Control					Reserved (0)					Sector Count (exp)					Sector Count								
4	Reserved (0)					Reserved (0)					Reserved (0)					Reserved (0)								

Fig. 12(i) Register FIS Host to Device

H-bll 91(ii)																					
0	Error				Status				R	I	R	Reserved (0)				FIS Type (34h)				90(ii)	
1	Dev / Head				Cyl High				Cyl Low								Sector Number				
2	Reserved (0)				Cyl High (exp)				Cyl Low (exp)								Sector Num (exp) (0)				
3	Reserved (0)				Reserved (0)				Sector Count (exp)								Sector Count				
4	Reserved (0)				Reserved (0)				Reserved (0)								Reserved (0)				

Fig. 12(ii) Register FIS Device to Host

																H-bit 91(iii)																	
0	Reserved (0)				Reserved (0)				R	R	R	Reserved (0)				FIS Type (39h)				90(iii)													

Fig. 12(iii) DMA Activate FIS, Device to Host

	H-bit																B1 (IV)																															
0	Reserved (0)								Reserved (0)								A	I	D	Reserved (0)								FIS Type (41h)								90(vi)												
1	DMA Buffer Identifier Low																																															
2	DMA Buffer Identifier High																																															
3	Reserved (0)																																															
4	DMA Buffer Offset																																															
5	DMA Transfer Count																																															
6	Reserved (0)																																															

Fig. 12(iv) DMA Setup FIS

																H-bit 91(v)																	
0	Error				R	Status Hi	R	Status Lo	R	I	R	Reserved (0)				FIS Type (A1h)				90(v)													
1	SActive 31:0																																

Fig. 12(v) Set Device Bits FIS

																H-bit 91(vi)						
0	Error				Status				R	I	D	Reserved (0)				FIS Type (5Fh)				90(vi)		
1	Dev / Head				Cyl High				Cyl Low				Sector Number									
2	Reserved (0)				Cyl High (exp)				Cyl Low (exp)				Sector Num (exp) (0)									
3	E_Status				Reserved (0)				Sector Count (exp)				Sector Count									
4	Reserved (0)								Transfer Count													

Fig. 12 (vi) PIO Setup FIS

Fig. 12 (vi) PIO Setup FIS

The diagram illustrates the structure of a PIO Setup FIS. It is a horizontal bar divided into several sections. The first section is labeled '0' and contains a 'Reserved (0)' field. This is followed by another 'Reserved (0)' field. Then, there are three 'R' fields. The next section is labeled 'H-bit' and '91(vii)' and contains a 'Reserved (0)' field. This is followed by a 'FIS Type (46h)' field. The final section is labeled '90(vii)' and contains 'N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)'. The diagram also shows a vertical axis on the left with labels '0', '...', '...', and 'n'.

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)	90(vii)
...								
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)							
n								

Fig. 12(vii) Data FIS

**Fig. 12(vii) Data FIS**

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Fig. 12 (viii) BIST Activate FIS

Fig. 12